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APPLICANTS	:	Manoj Khare et al.
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FOR	:	METHOD AND APPARATUS FOR REDUCING MEMORY LATENCY IN A CACHE COHERENT MULTI-NODE ARCHITECTURE
GROUP ART UNIT	:	2186
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AMENDMENT

S I R:

The following amendments and remarks below are respectfully submitted in response to the Office Action dated June 3, 2004.

IN THE CLAIMS:

Please amend the claims as follows (all claims listed):

1. (Previously Presented) A method for reducing memory latency in a multi-node architecture, comprising:

receiving a speculative memory read request at a home node before results of a cache coherence protocol are determined; and

initiating a read to memory to complete the speculative memory read request before results of the cache coherence protocol are determined.

2. (Currently Amended) The method of claim [[2]] 1, further comprising:

buffering results of the read to memory.

3. (Original) The method of claim 2, further comprising:

dropping the results of the read to memory on a buffer full condition or if a cancel command is received.

4. (Original) The method of claim 3, further comprising:

if a confirm command is received after results of the read to memory are dropped, initiating a second read to memory to complete a memory read request.

5. (Original) The method of claim 4, further comprising:

forwarding results of the second read to memory to a requester.

6. (Original) The method of claim 3, further comprising:

if a confirm command is received before results of the speculative read are dropped, forwarding the results of the read to memory to a requester.

7. (Original) The method of claim 6, wherein the speculative memory read request is issued by the requesting node.

8. (Original) The method of claim 6, further comprising:

receiving the results of the read to memory at the coherence agent; and

forwarding the results of the read to memory to the requesting node.

9. (Previously Presented) A method for reducing memory latency, comprising:

issuing a speculative memory read request to a home node before results of a cache coherence protocol are determined;

initiating a read to memory at said home node; and

initiating the cache coherence protocol after initiating the read to memory at said home node.

10. (Original) The method of claim 9, further comprising:

updating a memory status relating to the results in a table after the results of the cache coherence protocol are determined.

11. (Original) The method of claim 9, wherein initiating the cache coherence protocol comprising:

initiating a status look-up to determine the caching status of the requested memory.

12. (Original) The method of claim 11, further comprising:

issuing a confirm command to the home node if the caching status is determined to be in an invalid state or shared state.

13. (Original) The method of claim 11, further comprising:

snooping a node with the exclusive copy of the requested memory cached.

14. (Original) The method of claim 13, further comprising :

determining whether the exclusive copy of the requested memory is clean or dirty.

15. (Original) The method of claim 14, further comprising:

issuing a confirm command to the home node if the exclusive copy of the requested memory is clean.

16. (Original) The method of claim 14, further comprising:

issuing a cancel command to the home node if the exclusive copy of the requested memory is dirty.

17. (Original) The method of claim 13, further comprising:

receiving a snoop result, wherein the snoop result includes a copy of the requested memory; and

updating a memory status relating to the requested memory in a table.

18. (Original) The method of claim 17, further comprising:

receiving the requested memory; and

forwarding the requested memory to a requesting node.

19. (Previously Presented) A home node to respond to read requests in a multi-node architecture including a plurality of nodes, the home node comprising:

a processor;

a memory; and

a node controller coupled to the processor and memory, the node controller ~~adapted~~ to:

receive a speculative memory read request from a requester in the multi-node architecture before a cache coherence protocol is resolved, and

initiate a read to memory to complete the speculative memory read request before the cache coherence protocol is resolved.

20. (Original) The home node of claim 19 further comprising:

a buffer adapted to buffer the results of the read to memory.

21. (Original) The home node of claim 20, wherein the results of the read from memory are dropped from the buffer on a buffer full condition or upon receiving a cancel command.

22. (Original) The home node of claim 20, wherein the node controller responsive to a confirm is adapted to forward the results of the read to memory to the requester.

23. (Original) The home node of claim 20, wherein the node controller responsive to a cancel command is adapted to drop the data specified by the speculative read command.

24. (Previously Presented) A system comprising:

a node including a node controller to control a plurality of processors resident in the node, wherein the node controller is to receive a speculative read request before results of a coherence protocol are determined and the node controller is to read data specified by the speculative read command from memory before the results of the coherence protocol are determined; and

a coherence agent coupled to the at least one node, the coherence agent including a coherence controller adapted to determine the results of the coherence protocol and

adapted to forward a cancel command or a confirm command to the node after the results of the coherence protocol are determined.

25. (Original) The system of claim 24, wherein the node controller responsive to the confirm command issued by the coherence controller is adapted to send the data read from memory to the coherence controller.

26. (Original) The system of claim 24, wherein the node controller responsive to the cancel command issued by the coherence controller is adapted to drop the data read from memory.

27. (Original) The system of claim 24, further comprising:

a requesting node adapted to send a data read request to request data identified by a memory address included in the data read request.

28. (Original) The system of claim 27, wherein the speculative read request is sent by the requesting node.

29. (Original) The system of claim 24, wherein the speculative read request is sent by the switching agent.